EXHIBIT A

Expert Report on Monolithic Power Systems, Inc. v. O2 Micro International (Case C 08-4567 CW)

Dr. David J. Perreault

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14 June 2010

Introduction

Purpose of the report

This report concerns the case of *Monolithic Power Systems, Inc. v. O2 Micro International Ltd.,* Case No. C 08-4567 CW in the Northern District of California. As a court-appointed expert in this case, I have been asked to provide expert analysis and opinions regarding technical issues concerning validity/nonvalidity and infringement/noninfringement of the asserted claims of U.S. Patent No. 7,417,382 ("the '382 patent", attached as Appendix 1). These issues include:

- Whether any or all of the asserted claims (claims 1,2,4,7,8,9,11, and 14) of the '382 patent are invalid in view of the prior art, either due to anticipation or obviousness.
- Whether any or all of the accused products of Monolithic Power Systems, Inc. ("MPS"); ASUSTeK Computer Inc. and/or ASUS Computer International literally infringe the asserted claims of the '382 patent. These products include MPS products MP 1009; MP 1010B; MP 1026; MP 1038; and MP 1048 and ASUSTek/ASUS computer monitors and notebook computers that incorporate these MPS parts.

This report summarizes my assessment of these issues as of 14 June 2010. If/when deposed or asked to testify at trial, I expect to further elaborate and expand on the content of my report as necessary to make my testimony understandable to judge, jury and litigants. While I expect my testimony regarding these issues to be consistent with the content of this report, it should be understood that my assessment may change subsequent to this report in light of additional prior art or technical information that I subsequently review or recall or which is brought to my attention.

Qualifications

My name is David Perreault. I received the Bachelor of Science degree in Electrical Engineering (Summa Cum Laude) from Boston University in 1989. I received the Master of Science and Doctor of Philosophy (Ph.D.) degrees in Electrical Engineering from the Massachusetts Institute of Technology (MIT) in 1991 and 1997, respectively, with my doctoral research focused in the area of power electronics.

I joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate in 1997, and became a Research Scientist in the laboratory in 1999. Since 2001 I have been on the faculty of the MIT Department of Electrical Engineering and Computer Science, where I currently hold the position of Associate Professor with Tenure, and serve as the Chair of the Electronics, Computers, and Systems Area of the Department.

My research and development work has principally been in the field of power electronics, including the design, manufacturing, and control of power electronic circuits, and their use in a variety of applications. I teach the introductory circuits and electronics course as well as graduate-level power electronics courses at MIT, and am also a consultant to industry in the field. I have published a book chapter and more than 70 papers in the area of power electronics, hold 15 patents in the area, and have a number of others pending. I have also received a number of awards for my work in the field, including the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society and several prize paper awards.

I am a member of the Institute of Electrical and Electronics Engineers (IEEE), and a number of its societies including the Power Electronics Society, the Circuits and Systems Society, the Industrial Electronics Society, and the Industry Applications Society. I am presently a Member of the Power Electronics Society Administrative Committee. In addition, I am a reviewer for a number of conferences and journals, including the IEEE Energy Conversion Congress and Exposition, the IEEE International Symposium on Circuits and Systems, the IEEE Transactions on Power Electronics, and the IEEE Transactions on Circuits and Systems. I have served as associate editor for the IEEE Transactions on Power Electronics and on the technical program committee of several conferences. I consider myself to be an expert in the field of power electronics, and have been active in the field since well before the time of the patent in question (late 1990's). A copy of my Curriculum Vitae is attached as Appendix 2.

Materials Reviewed

To make an appropriate evaluation of the '382 patent and the accused products, I carried out a review of the prior art and information surrounding the '382 patent. This review encompasses a range of materials, including:

- A body of material relating to the prosecution and litigation of the '382 patent. This body of material, which was provided to me, includes patents, expert reports and associated exhibits, datasheets and application notes, product data, copies of circuit schematics, sections of technical books, and so forth.
- My personal collection of books, papers, and patents relating to the power electronics field.
- Books, trade publications, papers, patents and product data from the time period in question, including materials identified during a literature survey I carried out. The survey was not exhaustive.

The Practitioner of Ordinary Skill

In the field of the '382 patent, a practitioner having ordinary skill in the art would be a power electronics designer. Such a person typically has a bachelor's degree in Electrical Engineering, Physics, or a related discipline including relevant circuit design coursework, along with at least a couple of years of industry experience in designing power electronics. Such a person might alternatively have an advanced degree (such as a Master's degree in electrical engineering or a commensurate discipline) including coursework and/or project work in the area of power electronics along with at least a single year of industry experience in designing power electronics. I have used the above standard for a "practitioner of ordinary skill in the art" where necessary to my analysis.

Other Assumptions

In evaluating the `382 patent one must interpret the meanings of the words in the specification and the claims. Where needed, this report adopts the meanings and claim constructions construed by the United States District Court in its decision of February 16, 2010 (Appendix 3).

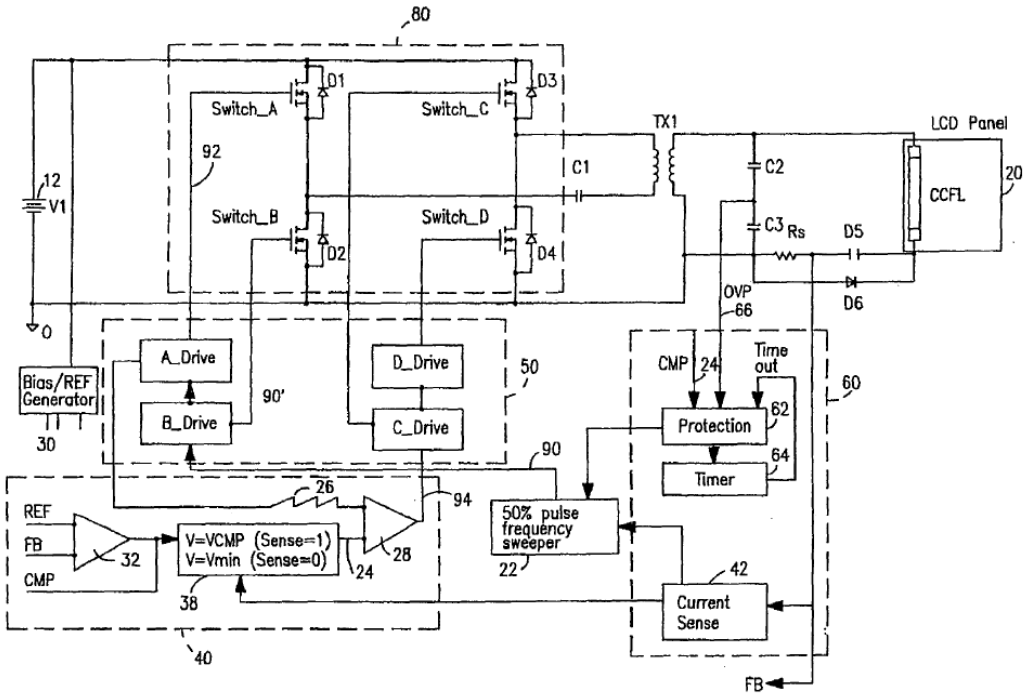

FIG. 2

Figure 1 This is Fig. 2 from US Patent 7,417,382 (the '382 patent).

In evaluating the art and product data provided to me, I sometimes must make assumptions about the relevant dates associated with that information in order to utilize it in my evaluation (e.g., I may take at face value the indicated date and revision number of a datasheet or application note.) This is necessary when I have no independent means of knowing the relevant date (or boundary on the date) with certainty. Likewise, I sometimes must make assumptions about the veracity of data or other information which I extract from reports (e.g., experimental data from an accused product). I try to clearly state where I make such assumptions, particularly where it may affect my conclusions. I would like to emphasize that my conclusions depend on the extent to which the cited information upon which I am relying is correct.

Background: the '382 Patent

In considering the '382 patent, it is useful to focus on those sections of the patent specification which is most important to the present dispute. One such section relates to overvoltage protection, and references Fig. 2 of the '382 patent (repeated here as Fig. 1). An important portion of the relevant text describing this part of the system is repeated here (Col 8 line40 to Col. 9 line 8):

> "To protect the circuit from an over-voltage condition, the present embodiment preferably includes protection circuit 60, the operation of which is provided below (the description of the over current protection through the current sense comparator 42 is provided above). The circuit 60 includes a protection comparator 62 which compares signal CMP with a voltage signal 66 derived from the load 20. Preferably, voltage signal is derived from the voltage divider C2 and C3 (i.e., in parallel with load 20), as shown in FIG. 2. In the open-lamp

> condition, the frequency sweeper continues sweeping until the OVP signal 66 reaches a threshold. The OVP signal 62 is taken at the output capacitor divider C2 and C3 to detect the voltage at the output of the transformer TXl. To simplify the analysis, these capacitors also represent the lump capacitor of the equivalent load capacitance. The threshold is a reference and circuit is being designed so that the voltage at the secondary side of the transformer is greater than the minimum striking voltage (e.g., as may be required by the LCD panel) while less than the rated voltage of the transformer. When OVP exceeds the threshold, the frequency sweeper stops the frequency sweeping. Meanwhile, the current-sense 42 detects no signal across the sense resistor Rs. Therefore the signal at 24, the output of a switch block 38, is set to be at minimum value so that minimum overlap between switches A,C and B,D is seen. Preferably, a timer 64 is initiated once the OVP exceeds the threshold, thereby initiating a time-out sequence. The duration of the time-out is preferably designed according to the requirement of the loads (e.g., CCFLs of an LCD panel), but could alternately be set at some programmable value. Drive pulses are disabled once the time-out is reached, thus providing safe-operation output of the converter circuit. That is, circuit 60 provides a sufficient voltage to ignite the lamp, but will shut off after a certain period if the lamp is not connected to the converter, so that erroneous high voltage is avoided at the output. This duration is necessary since a non-ignited lamp is similar to an open-lamp condition."

This is a very brief description of the architecture of the over-voltage protection (OVP) / open lamp circuitry. However, the description may be considered adequate, as this is a typical kind of function that might be implemented in such systems (see, e.g., [1-6]); it would easily understood by a practitioner of ordinary skill in the art, and could likewise be easily implemented (in many different ways) by a practitioner of ordinary skill. The facts that this architecture is easily understood and that its implementation is straightforward are underscored in the '382 specification (col. 10, lines 49-55):

> "Likewise, the protection circuit 62 and timer are constructed out of known circuits and are appropriately modified to operate as described herein. Other circuitry will become readily apparent to those skilled in the art, and all such modifications are deemed within the spirit and scope of the present invention, only as limited by the appended claims."

One point that may not be readily apparent to the uninitiated reader from the description (but would be understood by a practitioner of ordinary skill) relates to the voltage across the lamp (and consequently to the voltage processed through the capacitor divider for use in OVP). The voltage across the lamp is dominantly an alternating (ac) voltage at a (dynamically-varying) frequency determined by the driver circuitry (negligibly small dc components may also exist). Moreover its *amplitude* varies over time, according to the condition of the lamp and the control of the inverter circuit. The nature of the lamp voltage is illustrated qualitatively in Figure 2, with the voltage itself shown in red, and a representation of its amplitude shown in blue. The lamp voltage thus continuously swings through zero between positive and negative peaks as determined by its local amplitude.

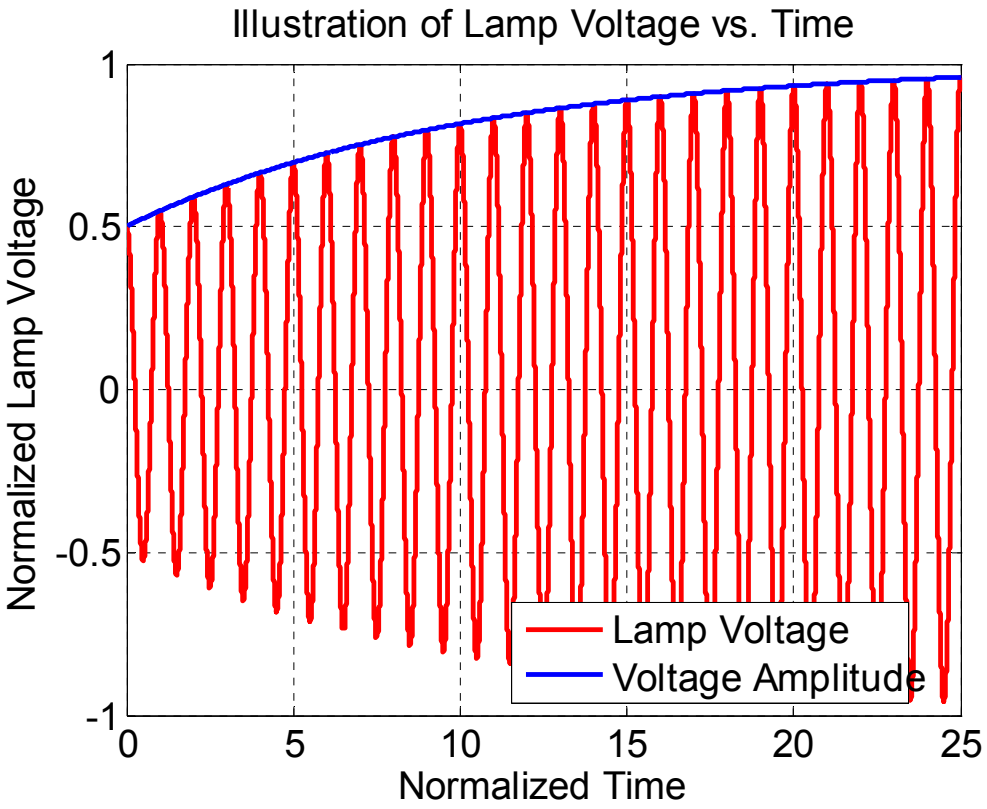

Figure 2 A qualitative representation of the voltage across the CCFL (item 20 in the diagram in Fig. 1).

Validity / Invalidity

This section addresses my evaluation of validity / invalidity of the individual claims of the patent.

Claim 1

Claim 1 of the '382 patent is as follows, with its individual elements broken out for clarity:

1.0	A DC to AC cold cathode fluorescent lamp inverter circuit, comprising:
1.1	A step-up transformer with a primary winding and a secondary winding for providing increased voltage to a cold cathode fluorescent lamp;
1.2	a first switch coupled to said step-up transformer for selectively allowing said step-up transformer to receive DC voltage of a first polarity;
1.3	a second switch coupled to said step-up transformer for selectively allowing said step-up transformer to receive DC voltage of a second polarity;
1.4	a capacitor divider electrically coupled to said cold cathode fluorescent lamp for providing a first voltage signal representing a voltage across said cold cathode fluorescent lamp;
1.5	a first feedback signal line coupled to said capacitor divider for receiving said first voltage signal from said capacitor divider representing said voltage across said cold cathode fluorescent lamp;
1.6	a timer circuit coupled to said first feedback signal line for providing a time-out sequence of a predetermined duration when said first voltage signal exceeds a predetermined threshold for said predetermined duration; and
1.7	a protection circuit coupled to said timer circuit, said first switch and said second switch for shutting down said first switch and said second switch after said predetermined duration.

Before evaluating validity/invalidity, it is important to understand how the claim language is construed. In my evaluation, I have adopted the claim construction provided by the court in its decision of February 16, 2010. Under this decision, the language of element 1.6 is construed as:

> "a timer circuit coupled to said first feedback signal line that measures a time period having a duration determined beforehand when the above-mentioned first voltage signal exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period"

Note that in interpreting this construction (or the language of element 1.6 itself), the meaning of the first voltage signal "exceeding" a voltage value must be understood in terms of the specification. In particular, it is not the *instantaneous* voltage but the *amplitude* of the voltage (or something related to it) that must have the characteristic "exceeds and continues to exceed a voltage value" in order that the system function as indicated in the specification. To understand this, recall that the instantaneous lamp voltage is dominated by its alternating (ac) component that oscillates through zero at a high rate (as illustrated in the red curve of Fig. 2). It is only the ac component of the lamp waveform which can be directly sensed through the capacitive divider, providing the "first voltage signal" (due to the frequency-dependent characteristics of a capacitor divider). Because the timer must operate over a longer time than a single cycle (as it may take numerous ac cycles for a lamp to "strike" or "ignite"), the *instantaneous* voltage itself cannot "exceed and continue to exceed" a value over a sufficiently long time. Rather, a signal related to some value such as the *amplitude* of the ac voltage (which also has units of voltage) must be considered (e.g., the blue curve of Fig. 2 as opposed to the red curve of Fig. 2), such that the signal "exceeds and continues to exceed a voltage value" for the needed duration of many cycles.

It is also notable that the specification and claims (and the construction of the claim language) do not specify the function or operation of the timer under all conditions of interest. For example, what the timer is supposed to measure / do when the "first voltage signal" exceeds the "voltage value" only intermittently (instead of continuously exceeding the voltage value for the above mentioned time period) remains undefined.

The MPS MP1010

The Monolithic Power Systems MP1010 and its associated application notes, data sheets and reference circuits is an important body of art to consider in assessing the validity / invalidity of the '382 patent. The MPS application note AN-01 v.10 dated February 1999 and the associated MPS datasheet v.2 dated February 1999 provide a reference design and associated explanation that is closely-related to the claimed art[1]. These documents, noted as reference numbers MONO-ITC-00116690-96 and MONO-ITC-00096731-736, are attached as Appendix 4 and Appendix 5, respectively. *In making this analysis I assume that this represents prior art to the '382 patent (which has a priority date of July 22, 1999).* For this section, I will refer to the version of the document in Appendix 4 as AN-01.

[1] I consider the application note and the datasheet together, since an application note would always be used in conjunction with the datasheet by an engineer. My conclusions would not change if the application note were considered on its own.

The application note introduction clearly states "A compact and efficient power inverter for driving a cold-cathode florescent lamp (CCFL) is implemented using the MP1010", thus satisfying element 1.0. Figure 3 shows both the MP1010 block diagram and the reference circuit design from the AN-01 reference. Considering the reference circuit and IC block diagram, it can be seen that the inverter system comprises a full-bridge inverter which is coupled through a transformer (step up transformer; recommended turns ratio of 1:100, as per AN-01 pg. 5). This immediately satisfies elements 1.1 through 1.3 of claim 1, leaving only elements 1.4 – 1.7 for discussion. I focus on these elements in more detail, as some of these elements have generated dispute in the present case.

Element 1.4 requires a capacitor divider electrically coupled to the CCFL. This capacitor divider is unambiguously provided by capacitors C10 and C11 in the "typical application circuit" (or "reference design"). The fact that C10 and C11 form a capacitor divider would be recognized by a person of ordinary skill in the art, and even by typical sophomore-level electrical engineering students. The fact that this pair of capacitors forms a divider is even referenced in the AN-01 text: "An open lamp timer can be implemented by feeding the lamp voltage back through a capacitive divider and a simple detector circuit", AN-01 pg. 4.

Element 1.4 also requires that the divider is "for providing a first voltage signal representing a voltage across said cold cathode fluorescent lamp". The "output node" of the divider formed at the junction of C10 and C11 certainly does this. The voltage at the output node is not a scaled version of the lamp voltage in all operating conditions, owing to the loading effects of the above-referenced detector circuit on the divider, but it is nonetheless representative of the voltage across the lamp (as it carries the needed information about the voltage across the lamp). Also clear is that the capacitor divider is loaded with the above-referenced detector circuit, formed with diode pair D1, resistor R3 and capacitor C9, such that the voltage on C9 has a relation to the lamp voltage amplitude for sufficiently large lamp voltage amplitudes. It is notable that the basic intent and operation of the circuit would be clear to one of ordinary skill in the art at the time in question. The effects of loading on divider circuits have long been taught at the undergraduate (typically sophomore) level in electrical engineering, and would certainly be recognized by a practitioner of ordinary skill in the art. Likewise, analysis of diode circuits and the operation of rectifiers and peak detectors are topics that are also typically taught at the undergraduate level (and have been, since long before the time of interest.) For example, Appendix 6 shows sections of undergraduate electronics textbooks (typically used at the sophomore and junior-year levels) describing the analysis and behavior of diode circuits in general and their application, including to detectors. In my opinion, there is no doubt that a practitioner of ordinary skill in the art would recognize that the reference circuit in AN-01 has a capacitor divider that provides a voltage signal representing the voltage across the lamp. The requirements of claim element 1.4 are thus clearly satisfied in my view.

Element 1.5 of claim 1 requires "a first feedback signal line coupled to said capacitor divider"; this is clearly provided by the connection from the above-mentioned divider output to the following circuitry for over-voltage protection. The use of this connection for feedback is confirmed by the fact that the voltage on this signal line is derived from the lamp voltage, and in turn influences operation of the circuit to affect lamp voltage.

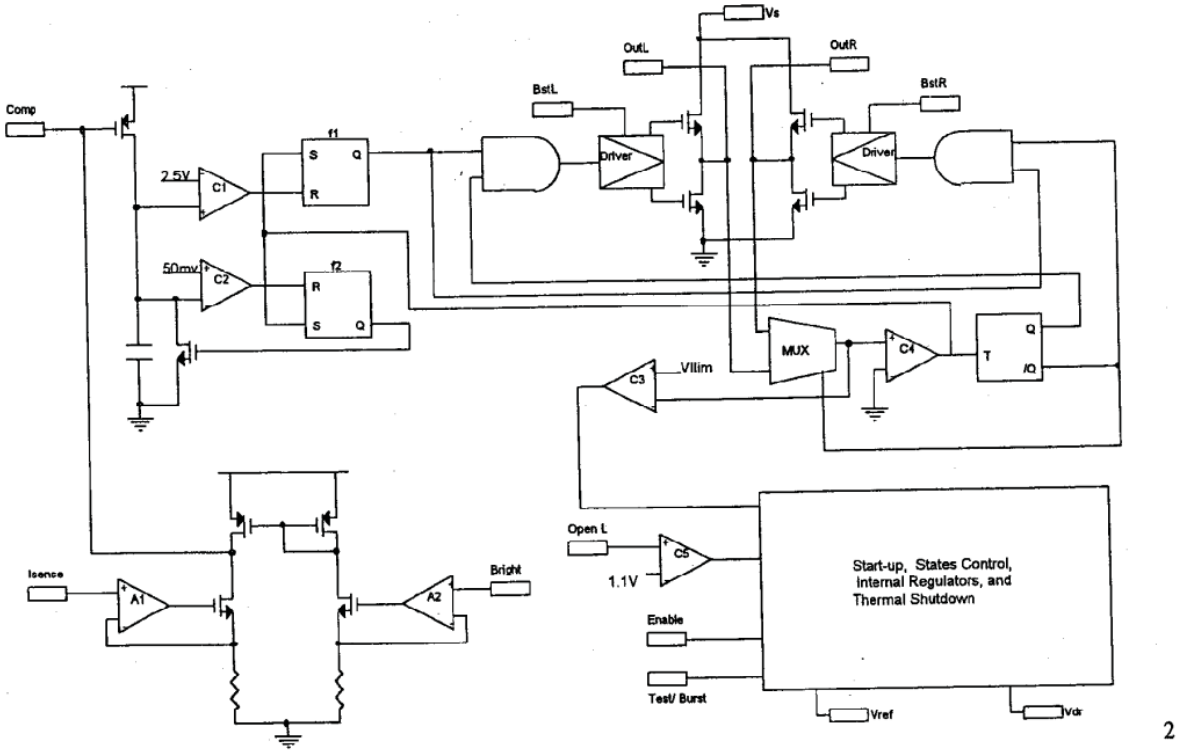

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Figure 2. Functional Block Diagram

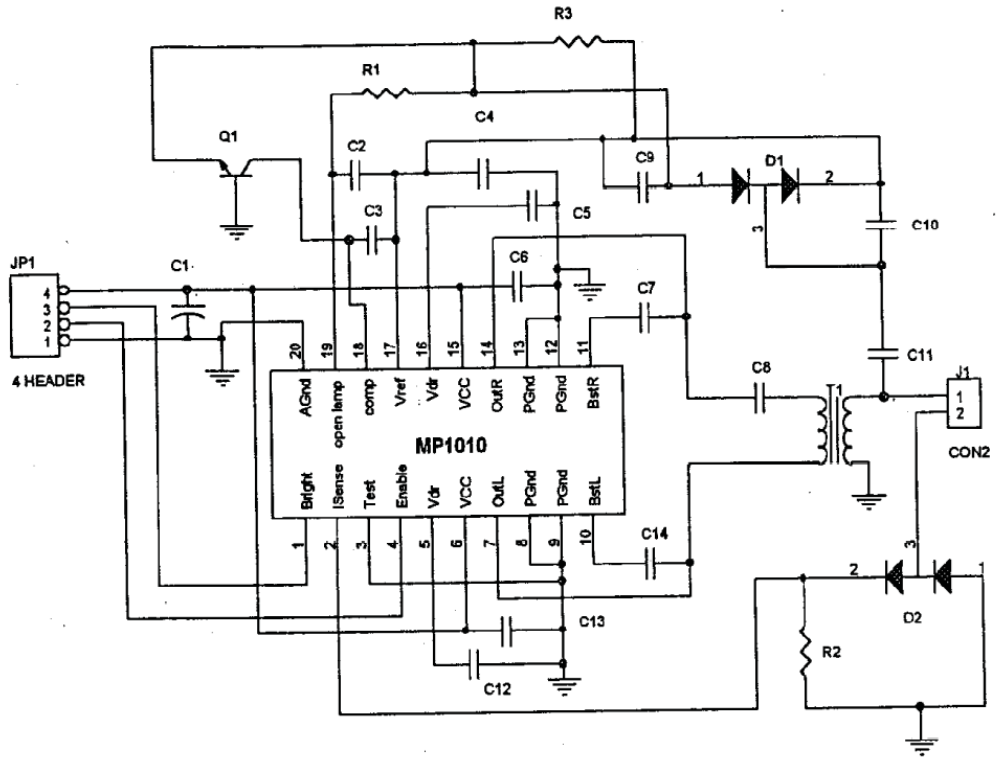

Figure 3. Typical Application Ciruit.

Figure 3 MP1010 block diagram and reference circuit design, as drawn from the MPS Application note AN-01 v.10, dated Feb. 1999 (Appendix 4). Connector Con-2 is indicated to connect to the CCFL as per AN-01 Figure 1.

As construed by the court, element 1.6 of claim 1 requires a timer circuit coupled to the feedback signal that "measures a time period having a duration determined beforehand when the above-mentioned first voltage signal exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period". As discussed in the background section, the first voltage signal "exceeding" needs to refer to a quantity other than instantaneous voltage (such as voltage amplitude) in order for the claim to make sense in the context of the specification. Here we examine the circuitry in the MP1010 reference circuit to evaluate its relation to the requirements of the claim element:

The circuitry connected to the capacitor divider in the reference circuit of AN-01 (with associated component values in the bill of materials) is clearly considered as a detector and open-lamp timer by the authors of AN-01, as stipulated in their description of page 4 (e.g., "an open lamp timer can be implemented by feeding the lamp voltage back through a capacitive divider and a simple detector circuit…") When the reference circuit is examined in conjunction with the component values indicated in the bill of materials and the text under "Open Lamp Protection" on page 4, the intended operation becomes clear (and, in my view, would have been clear to a practitioner of ordinary skill at the time). The detector circuit is clearly intended to operate such that for large lamp voltages, a voltage related to lamp voltage amplitude appears across capacitor C9, with fast (short time scale) adjustment for lamp voltage amplitude variations. Capacitor C2 is clearly intended to be used to provide a much longer time constant delay associated with the lamp timeout function. That is, capacitor C2, in conjunction with resistances in the circuit, provides a time delay in the change in voltage across C2 as compared to the voltage across C9 (and the lamp voltage amplitude), such that the comparator C5 at the "open lamp" pin of the MP1010 will trigger a shutdown only a significant time after lamp voltage amplitude has risen above an allowed amount. I would expect a practitioner of ordinary skill to recognize and understand these functions. I would also expect an ordinary practitioner to recognize that there is a degree of interaction among these functions (such that all of the component values C2, C9, R1, and R3 may influence the timer function to some degree depending on their values, as could interactions with the capacitor divider). I would also expect an ordinary practitioner to recognize that such interactions could be eliminated if desired through simple circuit modifications, and be able to carry out such circuit modifications were it deemed desirable.

The court's construction of claim element 1.6 requires a voltage that exceeds a "voltage value determined beforehand", i.e., a threshold. For lamp voltage amplitudes below a certain value, the reference circuit of AN-01 will function continuously (and never shut down). If the lamp voltage amplitude exceeds and remains above this same value, the comparator connected to the open lamp pin of the MP1010 will trigger and shut the system down in a finite amount of time that depends on the values of circuit components C2, C9, R1, and R3. This certainly represents a threshold, and based on the circuit and description provided, I would also expect an ordinary practitioner to recognize this. I would also expect an ordinary practitioner to be able to establish through hand analysis a rough approximation of this threshold (which depends on reference voltages internal to the MP1010 and the selection of the external component values of the timer), and readily determine a more exact value of the threshold through simulation if it was desired. I therefore conclude that there is a "voltage value determined beforehand".

The court's construction of claim element 1.6 also requires a timer circuit that "measures a time period having a duration determined beforehand." The authors of AN-01 certainly seek

to specify a predetermined time period before shutdown in their timing circuit. At the top of the first column of page 5 of AN-01, the authors state "Use the following equation to calculate the time set for open lamp shutdown count down timer", and specify an (approximate) shutdown time of R1*C2. It should be noted that this is only a crude approximation of the timeout delay under arbitrary operating conditions and component values. For relative component sizing similar to that in the bill of materials, the product of R1=R3 and C2 does control the time delay, but in general it can depend on all of the circuit components C2, C9, R1, and R3. More importantly, the time delay depends on the operating condition when the "open lamp" situation occurs: having an open lamp at startup would yield one delay, but a somewhat different delay would be found if the system was operating and the lamp was suddenly "removed" (e.g., due to breakage of a connection). Thus, the time delay will have a well-defined predictable value for the "usual" fault case of starting up in nominal conditions with an open lamp, but may be somewhat different for less usual conditions[2]. A key question regarding anticipation is whether this behavior is consistent with the requirement that the timer "measures a time period having a duration determined beforehand".

In my judgment, the reference circuit in AN-01 does meet the requirement that it "measures a time period having a duration determined beforehand", though I acknowledge that some engineers might draw a different conclusion based on how they interpret this requirement. I make this assessment based in part on the following: The '382 specification states (Col. 9, lines 4-8): "That is, circuit 60 provides a sufficient voltage to start the lamp, but will shut off after a certain period if the lamp is not connected to the converter". Under the fault condition the feature is designed to address (starting up without a lamp in place) a predetermined time period is indeed measured out by the AN-01 circuit[3]. Moreover, one can reach the same conclusion even considering other operating conditions (which yield some variation in lamp timeout duration) by recognizing that *all* practical timer systems have some degree of variation with operating condition (e.g., even a digital timer based on an oscillator will have measurable time variation with operating condition, owing to temperature sensitivity of the oscillator components among other factors.) The relevant engineering question is whether or not the accuracy is "sufficient unto the task". As the required accuracy of the timeout across operating conditions is not addressed anywhere in the '382 patent, one might reasonably infer that a moderate degree of variation under unusual operating conditions is acceptable.

The last detail of claim element 1.6 that should be discussed is the portion of the element that is construed as "when the above-mentioned first voltage signal exceeds and continues to exceed a voltage value". The operation of the AN-01 reference circuit is such that, under an open lamp condition, for example, the above-mentioned threshold IS exceeded. The function

[2] It may be useful for the non-engineering reader to consider an analogous situation that is more familiar. Consider the timing elements sometimes used in items such as dishwashers and toasters. These timers are often based on a simple "bimetallic strip", in which the time delay is set based on the strip bending out of shape and breaking a connection when it heats up (a "thermal time constant" instead of an "electrical time constant"). In the case when it has not been used for several minutes, a toaster incorporating a bimetallic strip timer might provide a relatively predictable, repeatable time for toasting a piece of bread. However, if the toaster is used multiple times in quick succession, the time might become shorter for later pieces of bread, owing to "preheating" of the bimetallic strip. Does such a timer "measure a time period having a duration determined beforehand"?

[3] I have not had the opportunity to personally test an actual circuit of the AN-01 reference design. However, because the system starts from a known state, and provides open-lamp voltage regulation (and thus repeatable average drive to the timer circuit during the timeout period), this conclusion is reasonable.

of transistor Q1 in the reference circuit is to provide feedback input to limit the peak-to-peak voltage amplitude applied to the lamp under open lamp conditions(and limit the divided-down voltage to a very approximate value of Vref + 3*Vd, as described in AN-01 pg. 4). This is higher than threshold voltage that will cause the MP1010 to shut down after the timeout. The exact threshold depends on component values, but could be very crudely approximated for the AN-01 reference circuit as Vref+2*Vd-V1.1, where V1.1 is the shutdown comparator trigger voltage (~1.1 V) and the other values are as defined in AN-01. The "exceeding" part is clear. One additional consideration for the AN-01 reference circuit and indicated component values is whether the action of Q1 will intermittently / transiently drive the sensed lamp voltage amplitude below the threshold during the timeout period under an open lamp condition. If this were true, operation would not meet the strict "continues to exceed" requirement for the specific case of open lamp operation and the indicated component values[4]. Since I have not had the opportunity to test an exact reference design, I cannot draw an absolute conclusion, though it is my *estimation* that this requirement would be met for this case (and it would certainly be met for other over-voltage operating conditions that did not trigger conduction of Q1)[5]. On this basis, it is my assessment that the AN-01 reference design timing circuit meets the requirement of claim element 1.6 in the '382 patent.

The final claim element 1.7 requires "a protection circuit coupled to said timer circuit, said first switch and said second switch for shutting down said first switch and said second switch after said predetermined duration." This is clearly provided in the AN-01 reference circuit. As described under "Open-Lamp Protection in AN-01, "If the voltage on the Open Lamp pin falls below the threshold, the MP1010 stops driving the load, turns off all four output switches, and disables the Drive regulator".

As described above, it is my assessment that the reference design presented in MPS application note AN-01 v.10 dated February 1999 meets the requirements of all elements of claim 1. To the extent that this represents prior art to the '382 patent, it is thus my assessment that claim 1 is *invalid by anticipation*. It is also my assessment that to the extent that the reference design of AN-01 is not found to anticipate claim 1, it certainly renders claim 1 obvious. That is, any differences between the ideas practiced in the AN-01 reference circuit and claim 1 of the '382 patent are such that the subject matter would have been obvious to a practitioner of ordinary skill at the time. The AN-01 circuit maps out the architecture presented in the '382 specification and claims down to a degree of simple design choices that would have been obvious to a practitioner of ordinary skill in the art at the time. The fact that these detailed selections represent obvious choices among well-understood alternatives is even reflected in the '382 specification (col. 10, lines 49-55):

> "Likewise, the protection
> circuit 62 and timer are constructed out of known circuits and
> are appropriately modified to operate as described herein.
> Other circuitry will become readily apparent to those skilled
> in the art, and all such modifications are deemed within the
> spirit and scope of the present invention, only as limited by

[4] For some circuit component selections of the AN-01 reference design, the "continues to exceed" requirement would certainly be met, but for this discussion I mainly focus on the EXACT design indicated in the AN-01 reference circuit including component values and types indicated in the bill of materials on pg. 7.

[5] If given the opportunity to test an AN-01 reference circuit, I could make a more definitive statement. However, I don't believe this is necessary to my conclusions. To the extent that the exact AN-01 reference circuit does not meet invalidity by anticipation, it certainly does so by obviousness, as described later.

> the appended claims."

There is no doubt in my view that claim 1 is *invalid by obviousness* in light of the art at the time, including the AN-01 reference circuit.

Claim 2

Claim 2 of the '382 patent is dependent on claim 1 and introduces a single new requirement, as follows:

> "…wherein said predetermined duration is sufficient for ignition of said cold cathode fluorescent lamp when properly operating."

Referring again to the above-referenced AN-01 document, this requirement would necessarily need to be met for the reference circuit design of AN-01 to be operable to drive a lamp from startup. (Otherwise, the circuit would time out and shut down without driving the lamp.) While I have not personally tested the reference circuit, it is reasonable to infer that it is operable. To the extent that a circuit of the reference design of AN-01 is operable, I assess that this claim is *invalid by anticipation*. Moreover, it would be obvious to a person of ordinary skill in the art reading the AN-01 application note that the duration of the timer must necessarily be set to enable the system to work properly, so even to the extent that the particular values shown in the reference design would not work in a particular instance, it would be obvious to a reader to modify them such that it would work. Thus, I assess this claim to also be *invalid by obviousness*.

Claim 4

Claim 4 of the '382 patent is also dependant on claim 1. It is shown as follows, with its individual elements broken out for clarity:

4.0	A DC to AC cold cathode fluorescent lamp inverter circuit as claimed in claim 1 further comprising:
4.1	a sense resistor electrically coupled to said cold cathode fluorescent lamp and electrically coupled to ground for providing a second voltage signal representing current through said cold cathode fluorescent lamp;
4.2	a second feedback signal line coupled to said sense resistor for receiving said second voltage signal from said sense resistor representing current through said cold cathode fluorescent lamp; and
4.3	a feedback control circuit coupled to said second feedback signal line for adjusting power to said cold cathode fluorescent lamp to a power level such that said second voltage signal approaches a reference value representing desired load conditions of said cold cathode fluorescent lamp.

Returning to the above-referenced AN-01, it can be seen that the new claim element 4.1 is certainly satisfied by resistor R2 in the typical application circuit. One end of the resistor is coupled to ground, while the other end is coupled to the lamp (through the diode rectifier / detector circuit D2 and connector Con2). The resistor develops a voltage whose average value is proportional to the amplitude of the lamp current (thus representing the lamp current). Resistor selection and operation of this portion of the reference circuit is described on page 3 of AN-01 under "Lamp Current Setting." The operation of this circuit for the purpose delineated in claim element 4.1 would also have been obvious to a practitioner of ordinary skill in the art at the time.

Claim element 4.2 is likewise satisfied by the connection from the "top" of resistor R2 to the Isense pin of the MP1010 in the reference circuit of AN-01.

Claim element 4.3 is likewise satisfied by the control circuitry illustrated in the "functional block diagram" and "typical application circuit" of AN-01, and the description of operation on pages 2 – 4 of AN-01. Operation of such analog feedback control circuitry would be familiar to practitioners of ordinary skill in the art. I thus conclude that claim 4 is likewise *invalid by anticipation*, and even if it were not would be *invalid by obviousness.*

Claim 7

Claim 7 of the '382 patent is also dependant on claim 1. It is shown as follows, with its individual elements broken out for clarity:

7.0	A DC to AC cold cathode fluorescent lamp inverter circuit as claimed in claim 1 further comprising:
7.1	a third switch coupled to said first switch and said step-up transformer for providing a first electrical path through said-up transformer to ground when said third switch and said first switch are simultaneously on;
7.2	a fourth switch coupled to said second switch and said step-up transformer for providing a second electrical path through said step-up transformer to ground when said fourth switch and said second switch are simultaneously on;
7.3	a sense resistor electrically coupled to said cold cathode fluorescent lamp and electrically coupled to ground for providing a second voltage signal representing current through said cold cathode fluorescent lamp;
7.4	a second feedback signal line coupled to said sense resistor for receiving said second voltage signal from said sense resistor representing current through said cold cathode fluorescent lamp; and
7.5	a feedback control circuit coupled to said second feedback signal line, said first switch and said third switch for adjusting time when said third switch and said first switch are simultaneously on such that said second voltage signal approaches a reference value representing desired load conditions of said cold cathode fluorescent lamp.

Of these elements, only 7.1, 7.2, and 7.5 are new relative to the above claims. Claim elements 7.1 and 7.2 are clearly satisfied by the full-bridge switch topology shown in the AN-01 "functional block diagram", and its connection to the transformer (via capacitor C8) illustrated in the "typical application circuit". Claim element 7.5 is also satisfied by operation of the control circuit indicated in the functional block diagram and described in the left column of page 3 of AN-01. Thus I thus conclude that claim 4 is likewise *invalid by anticipation* in light of the AN-01 document and reference circuit, and even if it were not, would be *invalid by obviousness*.

Claims 8, 9, 11, and 14

Claims 8, 9, 11, and 14 represent a second claim chain. These claims have essentially the same elements as the previously discussed claims, but focus on the application of the system outlined in claims 1-7 in "a liquid crystal display unit" comprising "a liquid crystal display panel" along with the previously claimed elements.

The above referenced document AN-01 described above with respect to invalidity of claims 1,2, 4, and 7 does not expressly describe combining the circuitry with a liquid crystal display

panel to build a liquid crystal display unit. However, the datasheet for the MP1010 (Appendix 5) clearly indicates this usage on page 1 under "Applications": "LCD backlight inverter for desktop or portable displays". Moreover, as backlights for such displays were a major application for such circuits at the time, it would have been obvious to an ordinary practitioner of the art at the time to apply the earlier-claimed circuitry with a liquid crystal panel to form a display unit. For example, consider the following references, all of which cite the use of ICs and circuits similar in purpose to that described in AN-01 for backlighting of display units:

[1]: "One of the central components in any active matrix LCD panel is the light source that is used to generate the light necessary for its operation. This light source consists of a cold cathode fluorescent lamp oftentimes abbreviated as CCFL. The power supply that drives this lamp is a low power high voltage inverter that operates around 35 to 70 kHz and is normally required to control the lamp current for brightness control."
[2]: "This paper describes a zero voltage switched (ZVS) resonant converter for driving cold cathode fluorescent lamps. Primarily intended for liquid crystal display (LCD) back-lighting, the circuit features…"
[3]: "The primary application is in inverters for cold-cathode fluorescent lamps ("CCFL"). Such lamps are widely used as backlight sources, for example in displays for notebook computers."

It may thus be concluded that claims 8, 9, 11, and 14 are at least *invalid by obviousness* in light of the AN-01 document and reference circuit and the widespread understanding of the field of use for such circuits.

Conclusion

Based on at least the AN-01 reference, it is my assessment that all of the asserted claims of the '382 patent are invalid, based on anticipation and/or obviousness, for reasons described above. I have only needed to use a portion of the relevant prior art to arrive at my conclusions. However, I would like to note that a significant body of other prior art can be used to support my conclusions about some or all of the asserted claims. Portions of this prior art are listed in the References section appended to this report. I reserve the right to support my conclusions with other prior art, including these references and other references brought up in litigation, if asked under deposition and/or at trial.

Infringement / Noninfringement

I have been asked to provide my opinion as to whether any or all of the accused products of Monolithic Power Systems, Inc. ("MPS"); ASUSTeK Computer Inc. and/or ASUS Computer International literally infringe the asserted claims of the '382 patent. These products include MPS products MP 1009; MP 1010B; MP 1026; MP 1038; and MP 1048 and ASUSTeK/ASUS computer monitors and notebook computers that incorporate these MPS parts.

In assessing literal infringement, I understand that I should identify whether each and every element of the asserted claims can be found in the accused MPS and ASUSTeK/ASUS products. In performing this analysis, it is clear that NONE of the ICs themselves literally

infringe any claims of the '382 patent, as they lack multiple elements required in the independent claims (1 and 8), including transformers and capacitive dividers. Consequently, I focus on assessing whether CCFL inverter circuits and LCD displays built with these ICs necessarily infringe or do not infringe, as the accused ASUSTeK/ASUS products purportedly utilize these ICs. Finally, I note that my assessment of infringement is made under the *assumption* that the claims being applied are valid, independent of my analysis as to whether or not they are valid.

MP1010B

In evaluating circuits built with the MPS MP1010B, I utilize information provided in the datasheet Rev 2.2, dated 3/3/2008 (MPS-ITC 000194 to 000203), as provided in the "Final Infringement Contentions" dated 3/25/2010.

In studying the datasheet for the MP1010B, the description of the fault protection circuitry provides a clue as to whether or not circuits built with this IC are likely to infringe the '382 patent. Page 7 of the datasheet, under "Fault Protection" reads:

> "Open Lamp: The OL Pin (#18) is used to detect whether an open lamp condition has occurred. A Capacitor divider (Cs1 and Cs2) is used to feedback the lamp voltage to OL with a DC bias of V_{REF} through Rs. During normal operation the OL pin is typically at 5V DC with an AC swing of less than 4V in amplitude. If an open lamp condition exists, the AC voltage on the OL line will swing below zero volts. When that occurs, the IC regulates the OL voltage to 10V p-p and a 1μA current source will inject into the FT pin. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

Important to the present discussion is how the open lamp regulation is indicated to work. Under the open lamp condition, this text indicates that the lamp voltage is regulated AT THE THRESHOLD which causes the shutdown timer to operate. This discussion suggests that the IC will not meet the requirement (e.g, of the court's construction of claim element 1.6) that the "first voltage signal exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period", since the "continues to exceed" condition (i.e., exceeds continuously) is not met. However, since the lamp voltage is indicated to be regulated *at the threshold* under this condition, a more detailed understanding of how the circuit operates is necessary to draw a definite conclusion.

In the "Rebuttal Expert Report of Aris K. Silzars" dated Aug. 25, 1999, a simplified diagram of the internal operation of the MP1015 is presented on pg. 25, and the report indicates that operation of the MP1010B is similar. The "final infringement contentions" of O2Micro (Exhibit A, pg. 19) utilize this figure as part of the contentions for infringement of circuits using the MP1010B. I therefore *assume* that this circuit accurately reflects the operation of the circuit in drawing my conclusions. I repeat the circuit diagram (from the final infringement contentions) as Fig. 4, and use it to evaluate the detailed operation of the MP1010B.

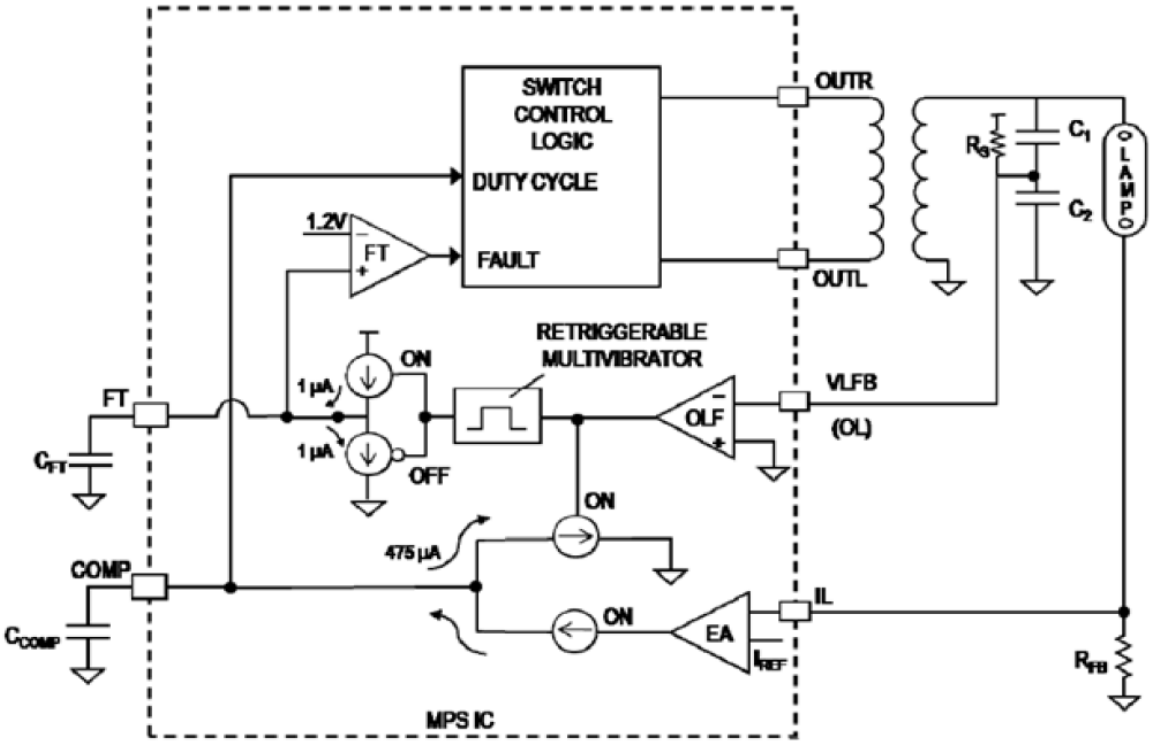

Figure 4 A simplified diagram of the internal operation of the MP1015, drawn from the "Rebuttal Expert Report of Aris K. Silzars" dated Aug. 25, 1999, and the "final infringement contentions" of O2Micro (Exhibit A, pg. 19). This simplified circuit diagram is assumed to represent the operation of other MPS ICs, including the MP1010B.

Examining the block diagram, it can be seen that the same comparator "OLF" that triggers the fault timer input is also used to regulate the voltage of the lamp under open-lamp conditions (by generating pulses of current drawn from the compensation capacitor Ccomp when the peak voltage excursion exceeds the threshold. The voltage on Ccomp in turn controls the lamp drive circuit, such that lamp voltage is temporarily reduced after a current pulse.) This operating strategy indicates that the amplitude of the sensed voltage will "limit cycle" about the threshold voltage that operates the timer. (That is, the lamp voltage amplitude will "jitter" between slightly above and slightly below the threshold during the open-lamp timeout period.) This description is consistent with the operation indicated in the datasheet. Importantly, this operating method fails to meet the requirements of the construed claims (e.g., claim element 1.6). The construction requires that the "first voltage signal exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period". Clearly, the voltage will not "continue to exceed" if the circuit operates as indicated. Rather, it will only "intermittently" exceed the voltage during the time-out duration, and will necessarily not exceed the threshold on some cycles.

I have not had the opportunity to personally test a circuit using the MP1010B. However, Dr. Silzars, in his above-mentioned rebuttal report does present test data asserted to be from an MP1010B, and this same data is utilized as support in the "Final Infringement Contentions". I therefore assume that this data accurately reflects the behavior of the circuit. One such plot drawn from the final infringement contentions (and well described in the Silzars report) is repeated here as Fig. 5. Because the same comparator is used both for pulling down the Ccomp voltage and for detecting a voltage exceeding the threshold, the Ccomp voltage behavior can be used to infer if the sensed voltage is "exceeding and continuing to exceed"

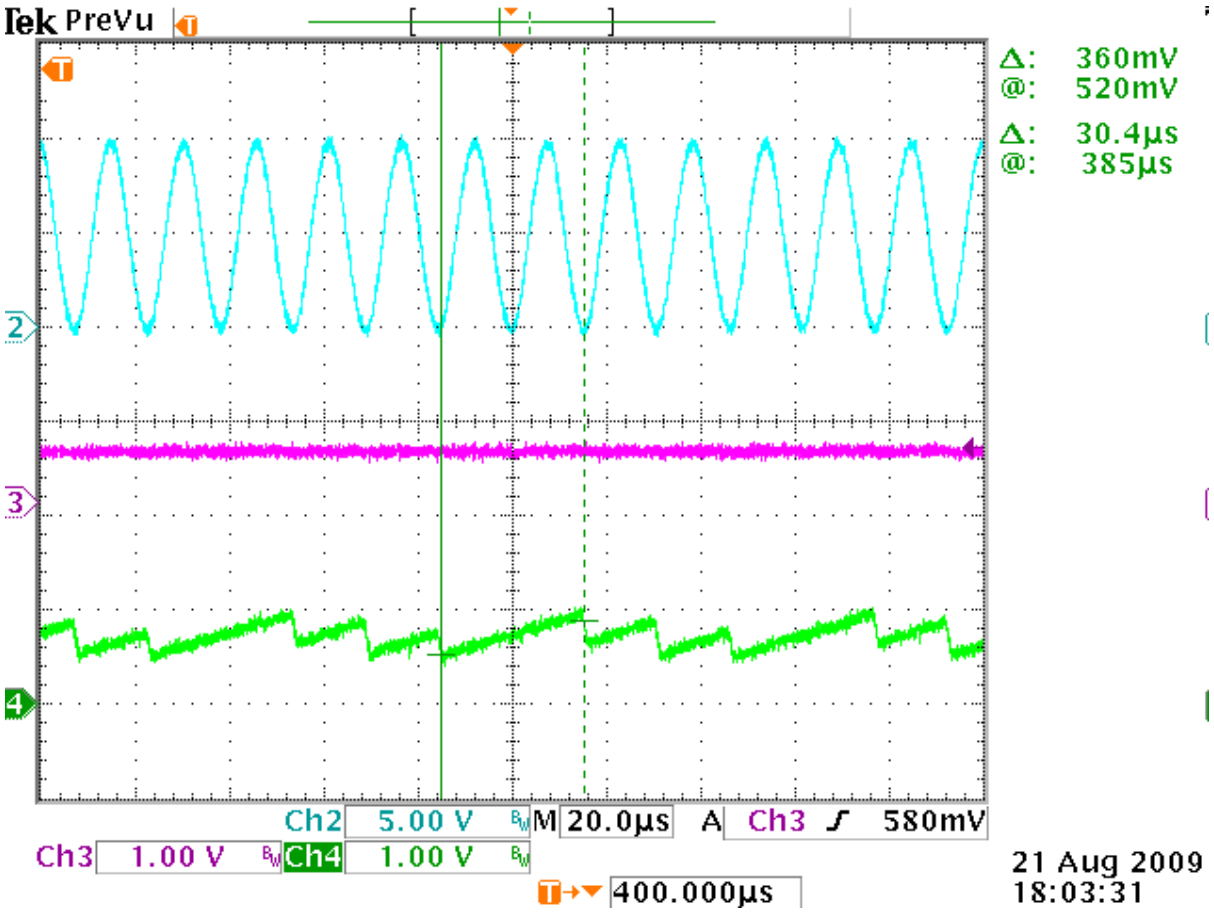

Figure 5 Scope trace illustrating operation of an MP1010B test circuit, drawn from the "Rebuttal Expert Report of Aris K. Silzars" dated Aug. 25, 1999 (Exh 135C), and the "final infringement contentions" of O2Micro (Exhibit A, pg. 19). This is assumed to well represent the operation of the MP1010B during an open lamp condition. The fact that channel 4 is pulled downwards on only a *subset* of ac cycles indicates that the detected voltage amplitude is indeed limit cycling both above and below the threshold voltage during the open lamp condition. It is thus *not* the case that the first voltage "exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period". This operation does not meet the construed claim requirement.

during the open lamp timeout. Channel 4 shows the Ccomp voltage during the open-lamp timeout. The fact that channel 4 is pulled downwards on only a *subset* of ac cycles indicates that the detected voltage amplitude is indeed limit cycling both above and below the threshold voltage during the open lamp condition. It is thus *not* the case that the first voltage "exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period". This operation does not meet the construed claim requirement.

Based on the above analysis and inferences from experimental results, I conclude that circuits built with the MP1010B IC will not infringe the claims of the '382 patent, at least because the "exceeds and continues to exceed" requirement of the claims as construed by the court is not met.

MP1026

As with the MP1010B IC, the product datasheet (rev. 1.6, 9/24/2007, MPS-ITC 000187 to 193) indicates that the open-lamp voltage will be regulated to the threshold voltage. Moreover, both the Silzars rebuttal report and the final infringement contentions cite the operation of the MP1026 as following the basic control method indicated in the circuit of Fig. 4. To the extent that this is true, I draw the same conclusion as for the MP1010B for the same reasons: circuits built with the MP1026 IC will not infringe the claims of the '382 patent, at least because the "exceeds and continues to exceed" requirement of the claims as construed by the court is not met.

MP1009

The fault protection circuitry of the MP1009 family (as described in the MP1009 datasheet Rev. 0.9, 10/17/2008, MPS-ITC 000164 to 174) is more sophisticated than that of the above ICs. The fault timer is triggered both by direct measurement of over-voltage and by measuring a lack of lamp current (datasheet pg. 6, under "Fault Protection"). Whether or not circuits built with this IC are likely to infringe is difficult to ascertain from the datasheet alone.

To make a more detailed assessment, I rely upon the "Proposed MP1009R1 Simplified Schematic" dated January 15, 2008 (Mono-ITC-00109612), which was presented to me with the "final infringement contentions", and is repeated here as Fig. 6. I make the *assumption* that this correctly reflects the operation of the produced MP1009 circuits. Multiple facts can be drawn from the simplified diagram. First, the "one shot" driving the fault timer is indeed triggered by more than just a voltage sense ("OR" of voltage and current inputs). Second, the comparator that sets the threshold and makes the "OV" (overvoltage) detection has several effects in the circuit in addition to driving the one-shot that operates the fault timer. Importantly, one of them is driving regulation of the lamp voltage under "open lamp" conditions. Thus, just as with the MP1010B described above, to the extent that the circuit diagram of Fig. 6 reflects operation of the MP1009, I expect that the regulation will be such that the "first voltage signal" will limit cycle about the overvoltage detect threshold. This operation does not meet the construed claim requirement.

This assessment is supported by experimental data presented in the above-referenced Silzars rebuttal report (pg. 34 and Exh. 135C), repeated here as Fig. 7. The fact that channel 4 is pulled downwards on only a *subset* of ac cycles indicates that the detected voltage amplitude is indeed limit cycling both above and below the threshold voltage during the open lamp condition. Variation in the "first voltage signal" of Channel 1 is consistent with this operation. To the extent that this data (of which I have no first-hand knowledge) correctly reflects operation of circuits built with MP1009 ICs under open-lamp operation, it is thus *not* the case that the first voltage "exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period".

Based on the above analysis and inferences from experimental results, I conclude that circuits built with the MP1010B IC will not infringe the claims of the '382 patent, at least because the "exceeds and continues to exceed" requirement of the claims as construed by the court is not met.

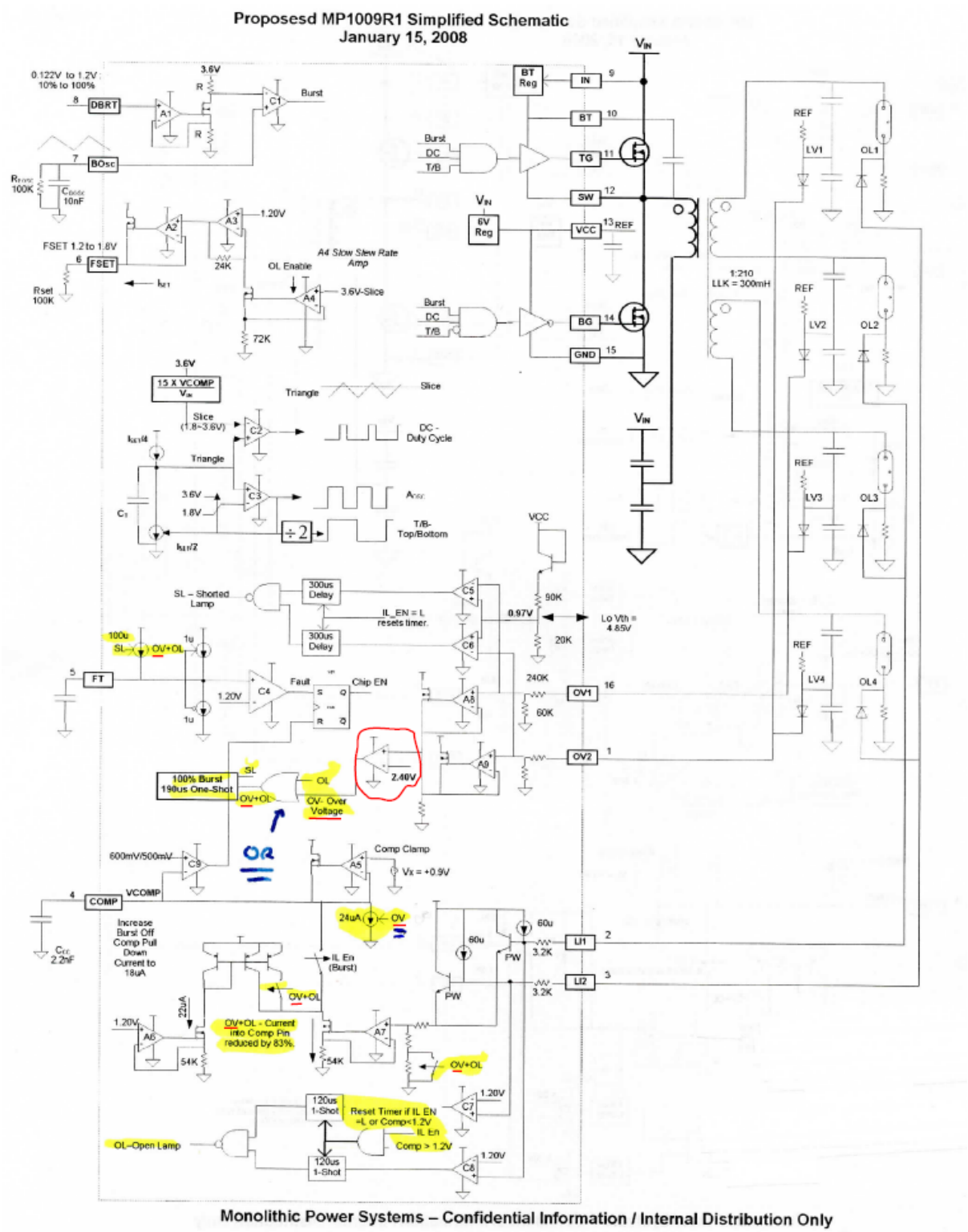

Figure 6 A simplified diagram of the internal operation of the MP1009R1, from the "Proposed MP1009R1 Simplified Schematic" dated January 15, 2008 (Mono-ITC-00109612), which was presented to me with the "final infringement contentions". For my analysis, I assume that this is a good representation of the operation of MP1009 devices. (Handwritten marks and highlighting are my own, added for emphasis.)

MP1038

In evaluating circuits built with the MPS MP1038, I utilize information provided in the datasheet Rev 1.9, dated 12/19/2005 (MPS-ITC 000152 to 000163), as provided to me with the "Final Infringement Contentions" dated 3/25/2010.

In studying the datasheet for the MP1038, the text describing fault protection is useful for assessing whether or not circuits built with this IC are likely to infringe the '382 patent. Page 8 of the datasheet, under "Fault Protection" reads:

> "Open Lamp: The LV Pin (#3) is used to detect whether an open lamp condition has occurred. If the voltage at LV exceeds +1.2V, a pulse of current will pull down on the COMP pin to regulate the lamp voltage. The Fault Timer will be started with a 1 μA current source injecting into C2 at the FT pin while the fault condition persists. If the voltage at the FT pin exceeds 1.2 V, then the chip will shut down.

Important to the present discussion is how the open lamp regulation is indicated to work. This suggests that, as with other MPS parts, the lamp is again regulated to the threshold voltage and will vary about it (both above and below the threshold) during an open lamp condition. I have no additional detail regarding the internal operation of the MP1038 circuitry to fully confirm whether or not this is true. If true, the MP1038 would not meet the claim requirements of the '382 patent as construed by the court for the same reasons as described above, and would not infringe. The data introduced in the above-referenced Silzars rebuttal report (Exh. 135D) appears consistent with "noninfringement", but without a view into the internal operation of the IC it is hard to make a conclusive judgment. Thus, it is my impression that it is unlikely that circuits based on the MP1038 will infringe the '382 patent, but I cannot make a definite conclusion on this point.

MP1048

In evaluating circuits built with the MPS MP1048, I utilize information provided in the datasheet Rev 0.9, dated 8/04/2006 (MPS-ITC 000175 to 000186), as provided to me with the "Final Infringement Contentions" dated 3/25/2010. The description of the open lamp fault protection in this datasheet (page 8, "open lamp" subsection of "Fault Protection") is identical to that of the MP1038. As with the MP1038, it is my *impression* that it is unlikely that circuits based on the MP1038 will infringe the '382 patent for reasons described in conjunction with the MP1038. However, I cannot make a definite conclusion on this point without additional information.

Conclusion

Based on the above analysis, it is my conclusion that circuits built with the MP1010B, MP1026, and MP1009 ICs will not infringe the '382 patent at least because the "exceeds and continues to exceed" requirement of the claims as construed by the court is not met. I cannot make definite assessments regarding the MP1038 and MP1048 ICs without additional information, but it is my impression that they will likely not infringe for at least the same reasons.

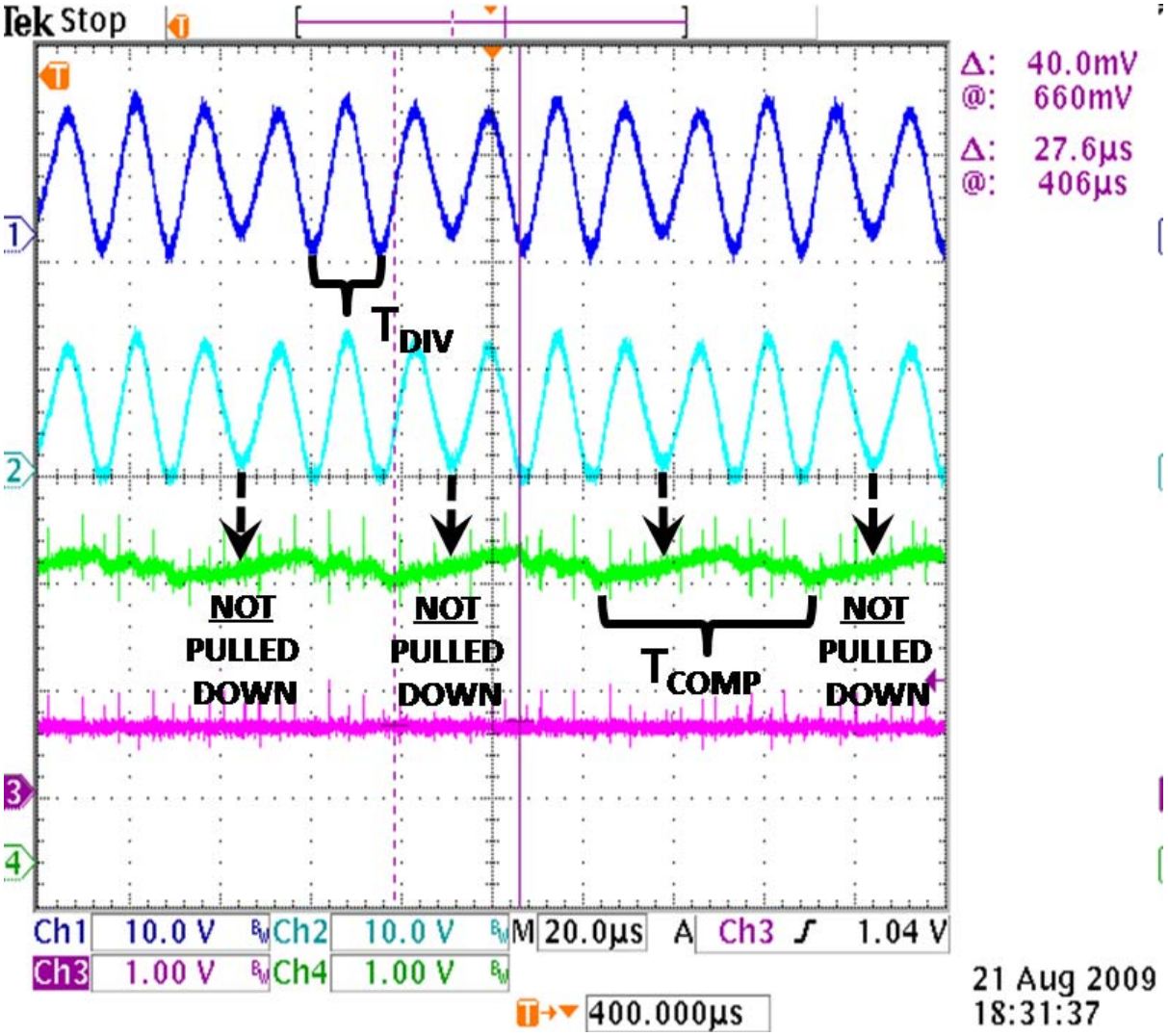

Figure 7 Scope trace illustrating operation of an MP10091 test circuit, drawn from the "Rebuttal Expert Report of Aris K. Silzars" dated Aug. 25, 1999 (Exh 135C). This is assumed to well represent the operation of the MP1009 during an open lamp condition. The fact that channel 4 is pulled downwards on only a *subset* of ac cycles indicates that the detected voltage amplitude is indeed limit cycling both above and below the threshold voltage during the open lamp condition. Variation in the "first voltage signal" of channel 1 is consistent with this operation. It is thus *not* the case that the first voltage "exceeds and continues to exceed a voltage value determined beforehand for the above-mentioned time period". This operation does not meet the construed claim requirement.

References

[1] M.K. Nalbant, "A New CCFL Inverter Circuit for AMLCD Panels Results In Significantly Higher Efficiency and Brightness," *AMLCDs '95*, pp. 133-136, 1995.

[2] M. Jordan and J.A. O'Connor, "Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution," *1993 IEEE Applied Power Electronics Conference*, pp. 424 – 431, Feb. 1993.

[3] R. Redl and K. Arakawa, "A Low-Cost Control IC for Single-Transistor ZVS Cold-Cathode Fluorescent Lamp Inverters and DC/DC Converters," *1997 IEEE Applied Power Electronics Conference*, pp. 1042 – 1049, Feb. 1997.

[4] Kawabata, et. al. "Information Processing Apparatus Including a Control Circuit for Controlling a Liquid Crystal Display Illumination Based on Whether Illuminatio Power Is Being Supplied From an AC Power Source or a Battery," *U.S. Patent 5,384,516.*, Jan. 24, 1995. (Kawabata '516).

[5] Nalbant, "Current Synchronous Zero Voltage Switching Resonant Topology," *U.S. Patent 5,615,093,* March 25, 1997. (Nalbant '093).

[6] Henry, "Apparatus and Method for Starting a Fluorescent Lamp" *U.S. Patent 5,923,129*, Jul. 13, 1999. (Henry '129).